AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-9 (canceled)

10. (Previously Added) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the ~~channel~~active, the structure comprising:

a thick insulating layer disposed over ~~the~~ said first and second trench, the thick insulating layer being conformal to ~~the~~ said first and second trench profile;

a gate electrode disposed over ~~the~~ said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion being embedded inside the first trench completely filling the first trench, the second vertical portion being embedded inside the second trench completely filling the second trench, and the horizontal portion being disposed over the substrate and connecting ~~the~~ said first and second vertical portions together; and

a first shallow doped region within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region disposed at an upper corner adjacent to the second portion of the electrode; and

a first deep source~~/drain junction~~ region extending from the first shallow doped region~~,~~ and a second deep ~~source/~~drain ~~junction~~ region are disposed in a region within the substrate deeper than the first and second trench.

11. (Previously Added) The structure according to claim 10, wherein the thick insulating layer is formed by thermal oxidation.

12. (Previously Added) The structure according to claim 10, wherein the thickness of the thick insulating layer is about 0.1 μm.

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13. (New) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thick insulating layer disposed over said first and second trench, the thick insulating layer being conformal to said first and second trench profile;

a gate electrode disposed over said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion being embedded inside the first trench, the second vertical portion being embedded inside the second trench, and the horizontal portion being disposed over the substrate and connecting said first and second vertical portions together; and

a first shallow doped region having dopants of first type within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region having dopants of first type disposed at an upper corner adjacent to the second portion of the electrode; and

a first deep source region having dopants of second type extending from the first shallow doped region and a second deep drain region having dopants of second type are disposed in a region within the substrate deeper than the first and second trench.

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14. (New) The structure according to claim 13, wherein the thick insulating layer is formed by thermal oxidation.

15. (New) The structure according to claim 13, wherein the thickness of the thick insulating layer is about 0.1 μm.

16. (New) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thick insulating layer disposed over said first and second trench, the thick insulating layer being conformal to said first and second trench profile;

a gate electrode disposed over said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion being embedded inside the first trench, the second vertical portion being embedded inside the second trench, and the horizontal portion being disposed over the substrate and bisecting said first and second vertical portions together; and

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a first shallow doped region within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region disposed at an upper corner adjacent to the second portion of the electrode; and

a first deep source region extending from the first shallow doped region and a second deep drain region are disposed in a region within the substrate deeper than the first and second trench.

17. (New) The structure according to claim 16, wherein the thick insulating layer is formed by thermal oxidation.

18. (New) The structure according to claim 16, wherein the thickness of the thick insulating layer is about 0.1 μm.

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Fig.2C. This sheet, which includes Fig. 2C, replaces the original sheet including Fig.2A-2C. In Figure 2C, previously having informal hand writing has been removed.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes